

FEATURES

- Optimized for Fiber Optic Photodiode Interfacing
- Eight Full Decades of Range
 - Low Conformance 0.1 dB from 1 nA to 1 mA
- Single-Supply Operation (3.0 V– 5.5 V)
- Complete and Temperature Stable
- Accurate Laser-Trimmed Scaling:
 - Logarithmic Slope of 10 mV/dB (at VLOG Pin)
 - Basic Logarithmic Intercept at 100 pA
 - Easy Adjustment of Slope and Intercept
- Output Bandwidth of 10 MHz, 15 V/ μ s Slew Rate
- 1-, 2-, or 3-Pole Low-Pass Filtering at Output
- Miniature 14-Lead Package (TS-SOP)
- Low Power: -4.5 mA Quiescent Current (Enabled)

APPLICATIONS

- High Accuracy Optical Power Measurement
- Wide Range Baseband Log Compression
- Versatile Detector for APC Loops

PRODUCT DESCRIPTION

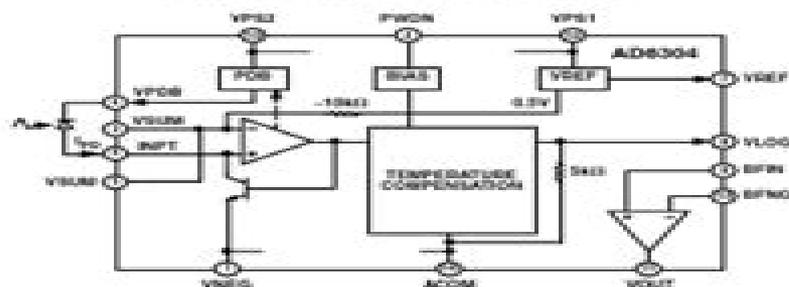
The AD8304 is a monolithic logarithmic detector optimized for the measurement of low frequency signal power in fiber optic systems. It uses an advanced translinear technique to provide an exceptionally large dynamic range in a versatile and easily used form. Its wide measurement range and accuracy are achieved using proprietary design techniques and precise laser trimming. In most applications only a single positive supply, V_{CC} , of 5 V will be required, but 3.0 V to 3.5 V can be used, and certain applications benefit from the added use of a negative supply, V_{EE} . When using low supply voltages, the log slope is readily altered to fit the available span. The low quiescent current and chip disable features facilitate use in battery-operated applications.

The input current, I_{PD} , flows in the collector of an optimally scaled NPN transistor, connected in a feedback path around a low offset JFET amplifier. The current-summing input node operates at a constant voltage, independent of current, with a default value of 0.5 V; this may be adjusted over a wide range, including ground or below, using an optional negative supply. An adaptive biasing scheme is provided for reducing the dark current at very low light input levels. The voltage at Pin VPDB applies approximately 0.1 V across the diode for $I_{PD} = 100$ pA, rising linearly with current to 2.0 V of net bias at $I_{PD} = 10$ mA. The input pin INPT is flanked by the guard pins VSUM that track the voltage at the summing node to minimize leakage.

REV. A

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FUNCTIONAL BLOCK DIAGRAM



The default value of the logarithmic slope at the output VLOG is accurately scaled to 10 mV/dB (200 mV/decade). The resistance at this output is laser-trimmed to 5 k Ω , allowing the slope to be lowered by shunting it with an external resistance; the addition of a capacitor at this pin provides a simple low-pass filter. The intermediate voltage VLOG is buffered in an output stage that can swing to within about 100 mV of ground (or V_{EE}) and the positive supply, V_{CC} , and provides a peak current drive capacity of ± 20 mA. The slope can be increased using the buffer and a pair of external feedback resistors. An accurate voltage reference of 2 V is also provided to facilitate the repositioning of the intercept.

Many operational modes are possible. For example, low-pass filters of up to three poles may be implemented, to reduce the output noise at low input currents. The buffer may also serve as a comparator, with or without hysteresis, using the 2 V reference, for example, in alarm applications. The incremental bandwidth of a translinear logarithmic amplifier inherently diminishes for small input currents. At the 1 mA level, the AD8304's bandwidth is about 2 kHz, but this increases in proportion to I_{PD} up to a maximum value of 10 MHz.

The AD8304 is available in a 14-lead TS-SOP package and specified for operation from -40°C to $+85^{\circ}\text{C}$.

160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic

Hussin A.Rothana



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160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic Book Review: Unveiling the Power of Words

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Table of Contents 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic

1. Understanding the eBook 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - The Rise of Digital Reading 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Advantages of eBooks Over Traditional Books
2. Identifying 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - User-Friendly Interface
4. Exploring eBook Recommendations from 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Personalized Recommendations
 - 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic User Reviews and Ratings

- 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic and Bestseller Lists
- 5. Accessing 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic Free and Paid eBooks
 - 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic Public Domain eBooks
 - 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic eBook Subscription Services
 - 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic Budget-Friendly Options
- 6. Navigating 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic eBook Formats
 - ePub, PDF, MOBI, and More
 - 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic Compatibility with Devices
 - 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Highlighting and Note-Taking 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Interactive Elements 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
- 8. Staying Engaged with 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
- 9. Balancing eBooks and Physical Books 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Setting Reading Goals 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Fact-Checking eBook Content of 160 Db Range 100 Pa To 10 Ma Low Cost Logarithmic
 - Distinguishing Credible Sources

13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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