

Top-down delayering by low energy, broad-beam, argon ion milling – a solution for microelectronic device process control and failure analyses

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We describe a new delayering solution for semiconductor quality control and failure analyses using low-energy, broad-beam argon ion milling. The results show a large, delayered area, suitable for high resolution scanning electron microscopy (SEM) investigation and energy dispersive X-ray spectroscopy (EDS) characterization. The technique allows full top-down delayering, layer by layer, of three-dimensional vertical NAND (3D V-NAND) flash memory devices. We show that it is possible to stop at each device layer and carry out observation and characterization. Furthermore, we demonstrate that the technique does not introduce any additional damage to the device being investigated.

Keywords – failure analysis; flash memory; ion milling; top-down delayering; delayering

I. INTRODUCTION

The semiconductor industry is a dynamic, rapidly growing manufacturing sector. In 2015, global sales of semiconductor products increased 9.9% and reached a record US \$335.8 billion [1]. Constantly evolving microelectronic device designs continue to grow more complex, more compact, and smaller – reaching nanoscale. For example, 3D V-NAND flash memory cells are layered vertically in three-dimensional stacks, which provides much greater cell density and increases memory capacity [2]. Such design complexity makes maintaining manufacturing quality standards a consistent challenge for the industry and failure analysis (FA) plays a critical role in meeting that challenge. Process control and FA can determine the root cause of a defective device; they enable failure identification and characterization, as well as provide feedback for product and process improvement.

Many failure analysis techniques, both nondestructive and destructive, have been developed in the past five decades [3, 4]. Nondestructive techniques include electrical measurement and testing, infrared and X-ray examination, and optical or electron microscopy evaluation. Destructive techniques include chemical etching, mechanical polishing, plasma etching, and delayering. Many techniques are unfeasible for multilayer devices. For example, Samsung found that etching agents are too aggressive and the company enumerated several major structural failures that can occur in NAND flash memory related to etching or particle contamination [5]. Delayering is a

popular choice because it allows top-down, whole chip characterization. The primary challenge presented by a vertical stack is looking through many dissimilar layers. FA often requires the ability to investigate different layers simultaneously [6]. A top-down delayering process that employs conventional mechanical preparation techniques has been documented as a challenging and difficult to control process that does not allow targeting of a specific depth or layer [6, 7]. Gallium- and xenon-based focused ion beam (FIB) techniques have been used for delayering of semiconductor devices [6, 8, 9]. However, in addition to causing curtaining and redistribution problems, its most important limitation is delayering of relatively small area: about 20 x 20 μm for Ga FIB [6] and about 100 x 100 μm for Xe FIB [9, 10]. That limitation makes it impossible to use a FIB system to prepare a large, sloped area that exposes all the layers simultaneously. Therefore, there is a need to develop a precise, fast, and relatively simple delayering process that overcomes these limitations.

Unlike FIB-based techniques, broad-beam argon ion milling does allow the uniform removal of large areas of material significantly greater than 100 μm , which is suitable for microelectronics layer-by-layer investigation. It enables a precise and controlled delayering process that yields a large, sloped area that allows observation of all layers simultaneously. This paper presents a new development in semiconductor device delayering for FA that uses low energy, broad-beam argon ion milling.

II. EXPERIMENT

The experiment was performed on commercially available Samsung 3D V-NAND flash memory. This device was chosen because its elaborate structure better demonstrates the delayering technique, not because of a defect investigation.

NAND (Fig. 1) is a logic gate that has two inputs, each of which can be true or false. A NAND gate produces true output only if at least one of the two operands is false, or produces false output only if all its inputs are true. Data retention in a NAND cell is based on charge trap effect, i.e., electrons are stored in silicon nitride layer [13, 14].

Microelectronic Device Delaying Using Note Fischione

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