

# Defect Detection with Transient Current Testing and its Potential for Deep Sub-micron CMOS ICs

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## Abstract

*Transient current testing ( $I_{DDT}$ ) has been often cited as an alternative and/or supplement to  $I_{DDQ}$  testing. In this article we investigate the potential of transient current testing in faulty chip detection with silicon devices. The effectiveness of the  $I_{DDT}$  test method is compared with  $I_{DDQ}$  as well as with  $Sb$ -based voltage testing. Photon emission microscopy is used to localize defects in several faulty devices. Furthermore, the potential of  $I_{DDT}$  testing for leaky deep sub-micron devices is investigated.*

## 1 Introduction

Quiescent current testing ( $I_{DDQ}$ ) is an important ingredient of the test suite for digital VLSI. The contributions of  $I_{DDQ}$  testing in quality improvement, test cost reduction, burn-in elimination have been well recognized [1]. However, the effectiveness of conventional  $I_{DDQ}$  testing in deep sub-microns is expected to be eroded owing to the increased sub-threshold current in MOS transistors [2-5]. Many solutions have been proposed to contain the increased sub-threshold leakage and are documented elsewhere [3,5,6]. These solutions include utilization of reverse biasing techniques to reduce the sub-threshold leakage in the test mode [3,5], utilization of Silicon On Insulator (SOI) technology for a steeper sub-threshold swing [7,8], or utilization of multi-threshold transistors to contain the sub-threshold leakage [9]. Moreover, containment of sub-threshold leakage is an important parameter for low power and device reliability consideration. Therefore, many low power circuit-level techniques have been devised to significantly reduce the sub-threshold leakage current.

Typically these solutions require non-trivial changes in the standard cell library or in the process. In many applications such as high performance VLSI, these solutions may pose several restrictions. CMOS processes for such devices are aggressively scaled ( $V_T$  and gate oxide) and optimized for switching speed. As a result, these devices are not  $I_{DDQ}$  testable. Therefore, ensuring gate oxide quality and reliability is becoming an increasingly difficult as well as an expensive task.

In this article, we investigate the potential of transient current testing ( $I_{DDT}$ ) as an alternative/supplement to  $I_{DDQ}$  testing. The motivation of this research comes from the following reasons: (i) To compare the effectiveness of  $I_{DDT}$  with respect to  $I_{DDQ}$  and voltage testing. For a production test method, the reproducibility of the test method is of prime importance. (ii) To investigate the feasibility of  $I_{DDT}$  based test techniques in a deep sub-micron environment. Current-based test techniques are much more sensitive compared to voltage-based counter parts. Owing to several factors, in deep sub-micron voltage-based test strategies are unlikely to guarantee quality expectations. (iii) To investigate the speed-up factor. For  $I_{DDQ}$  measurements, one does not have to wait till the current has reached the quiescent level. Hence, it is possible to enhance speed of the measurements. In other words, it is possible to perform  $I_{DDT}$  measurements at a significantly higher rate compared to  $I_{DDQ}$  measurements.

## 2 Previous Work

Some of the initial work on  $I_{DDT}$  was done by Frenzel and Marinus [10]. They simulated a small TTL circuit (few logic gates) assigning different sinusoidal waveforms on the inputs. They described complete power supply current as a signature of the Device Under Test (DUT). The signature of the DUT was compared with that of a golden device. In this manner a pass/fail criterion was established. So and Misaki [11] applied dynamic current monitoring techniques on SRAMs. To improve the defect detection capabilities of the dynamic current, they incorporated an extensive DFT strategy. The DFT scheme included separate  $V_{DD}$  and  $V_{SS}$  supplies for transient measurements, distributed switches to switch between the normal  $V_{DD}$  ( $V_{DD}$ ), and a test  $V_{DD}$  ( $V_{DD}$ ) only for dynamic current measurements. Furthermore, two dynamic current monitors and a set of controls are needed on the DUT. In their subsequent paper [12], the authors implemented the concept in silicon. The results reported showed that  $I_{DDT}$  is a better test method compared to  $I_{DDQ}$  and logic testing for open defects. However, the DFT implementation required is non-trivial and has implications for performance and test overhead.

Musipacific et al. [13] proposed the concept of Transient

# Defect Detection With Transient Current Testing And Its

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### **Table of Contents Defect Detection With Transient Current Testing And Its**

1. Understanding the eBook Defect Detection With Transient Current Testing And Its
  - The Rise of Digital Reading Defect Detection With Transient Current Testing And Its
  - Advantages of eBooks Over Traditional Books
2. Identifying Defect Detection With Transient Current Testing And Its
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Defect Detection With Transient Current Testing And Its
  - User-Friendly Interface
4. Exploring eBook Recommendations from Defect Detection With Transient Current Testing And Its
  - Personalized Recommendations
  - Defect Detection With Transient Current Testing And Its User Reviews and Ratings
  - Defect Detection With Transient Current Testing And Its and Bestseller Lists

5. Accessing Defect Detection With Transient Current Testing And Its Free and Paid eBooks
  - Defect Detection With Transient Current Testing And Its Public Domain eBooks
  - Defect Detection With Transient Current Testing And Its eBook Subscription Services
  - Defect Detection With Transient Current Testing And Its Budget-Friendly Options
6. Navigating Defect Detection With Transient Current Testing And Its eBook Formats
  - ePub, PDF, MOBI, and More
  - Defect Detection With Transient Current Testing And Its Compatibility with Devices
  - Defect Detection With Transient Current Testing And Its Enhanced eBook Features
7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Defect Detection With Transient Current Testing And Its
  - Highlighting and Note-Taking Defect Detection With Transient Current Testing And Its
  - Interactive Elements Defect Detection With Transient Current Testing And Its
8. Staying Engaged with Defect Detection With Transient Current Testing And Its
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Defect Detection With Transient Current Testing And Its
9. Balancing eBooks and Physical Books Defect Detection With Transient Current Testing And Its
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Defect Detection With Transient Current Testing And Its
10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
11. Cultivating a Reading Routine Defect Detection With Transient Current Testing And Its
  - Setting Reading Goals Defect Detection With Transient Current Testing And Its
  - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Defect Detection With Transient Current Testing And Its
  - Fact-Checking eBook Content of Defect Detection With Transient Current Testing And Its
  - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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current exam list cisco - Oct 14 2022

web cisco certification exams current exams passing one or more exams is the requirement for achieving certification and in most cases for recertification the following list identifies all currently available exams by certification and track in some cases different tracks may require the same exam