

3.8 See Figure S.8. The rename table has arbitrary values at clock cycle  $N - 1$ . Look at the next two instructions (I0 and I1): I0 targets the F1 register, and I1 will write the F4 register. This means that in clock cycle  $N$ , the rename table will have had its entries 1 and 4 overwritten with the next available Temp register designators. I0 gets renamed first, so it gets the first T reg (9). I1 then gets renamed to T10. In clock cycle  $N$ , instructions I2 and I3 come along; I2 will overwrite F6, and I3 will write F0. This means the rename table's entry 6 gets 11 (the next available T reg), and rename table entry 0 is written to the T reg after that (12). In principle, you don't have to allocate T regs sequentially, but it's much easier in hardware if you do.

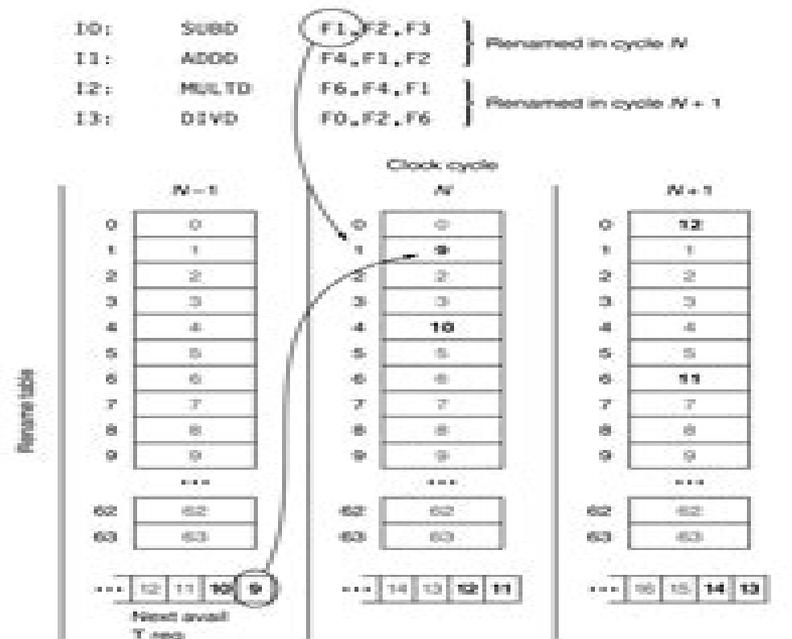


Figure S.8 Cycle-by-cycle state of the rename table for every instruction of the code in Figure 3.51.

3.9 See Figure S.9.

ADD	R1, R1, R1;	5 + 5 → 10
ADD	R1, R1, R1;	10 + 10 → 20
ADD	R1, R1, R1;	20 + 20 → 40

Figure S.9 Value of R1 when the sequence has been executed.

# Computer Architecture A Quantitative Approach Solution 5

**SA Dillow**



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